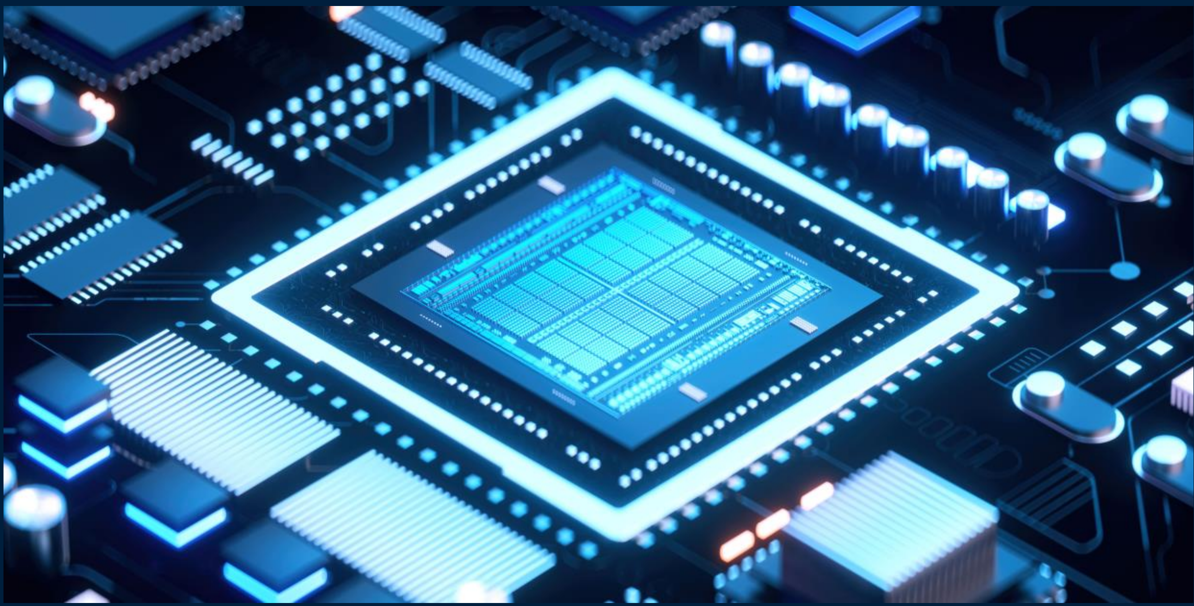
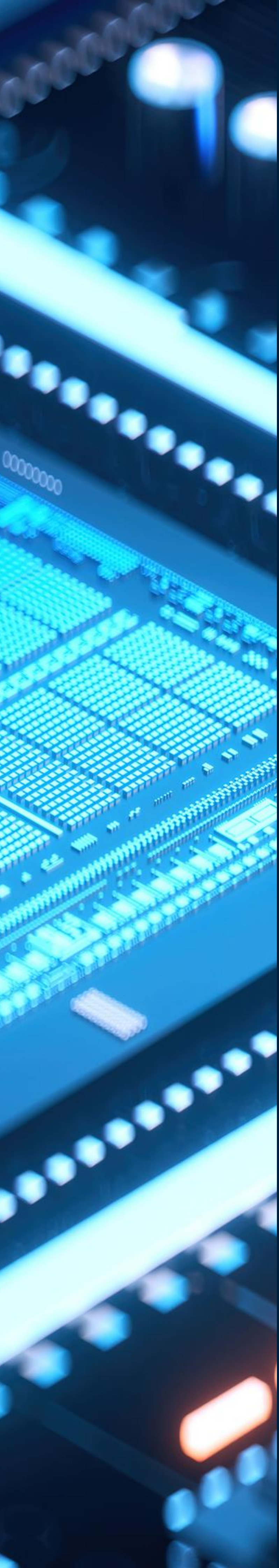


Latest Trends in Core Materials Supporting Next-Generation Semiconductor Packages and Substrates



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1. Introduction

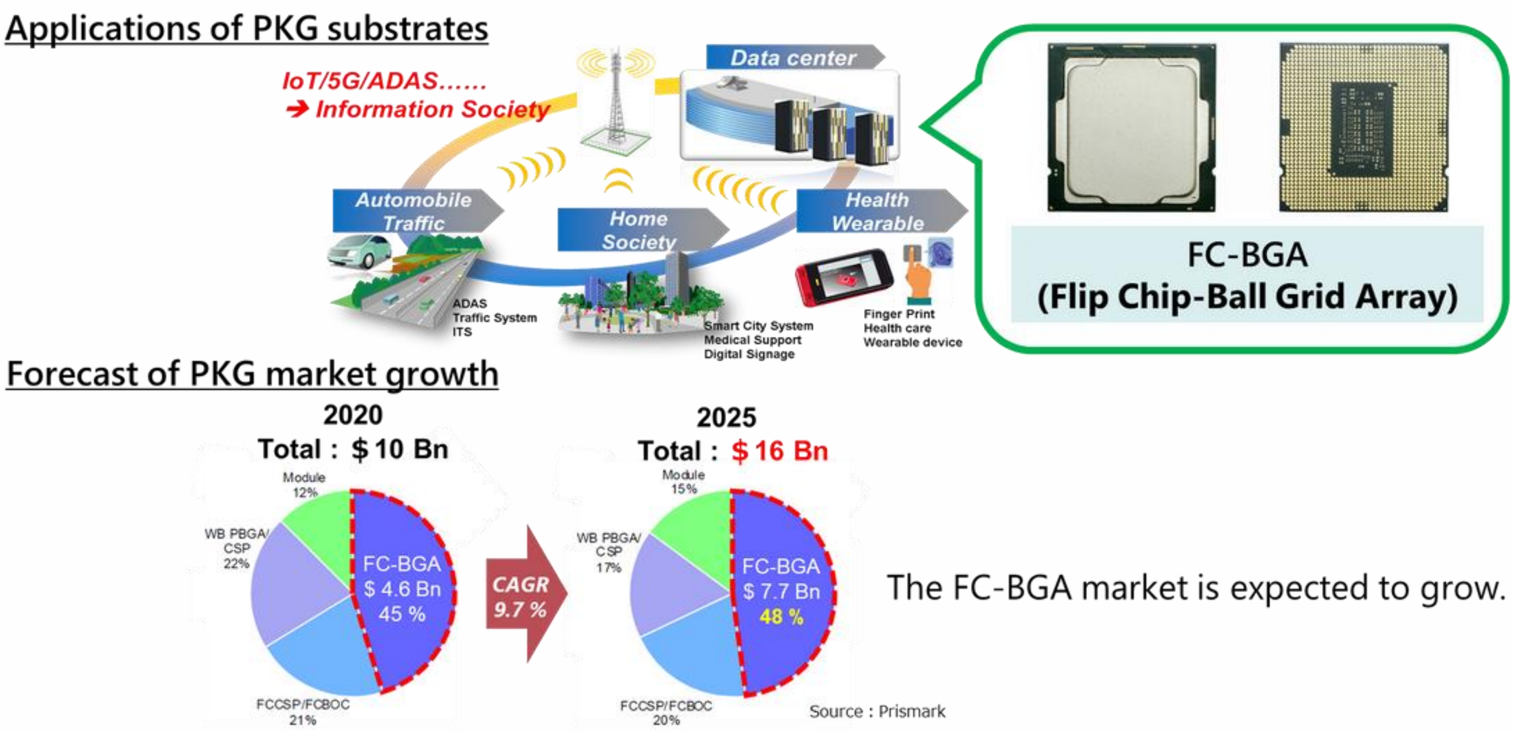
As the volume of information explodes with the widespread use of the Internet of Things (IoT), 5G networks, advanced driver-assistance systems (ADAS), and generative artificial intelligence (AI), information processing devices for data centers and terminals require the capability to transmit information more quickly in larger volumes and wider bandwidths. Accordingly, the demand for more finely pitched, highly integrated and densely packed semiconductor chips is rising, while package substrates require larger areas and narrower pitches for pitch connections to facilitate the mounting of multiple devices, and even to accommodate future 2.xD to 3D packages.

This article examines the latest trends in core materials supporting next-generation semiconductor packages and substrates, and introduces Resonac's newest low-warpage, low CTE (coefficient of thermal expansion), and high elastic modulus core material MCL-E-795G and TYPE-F technology for high thickness accuracy.

2. Market and technology trends

01 | MARKET TRENDS

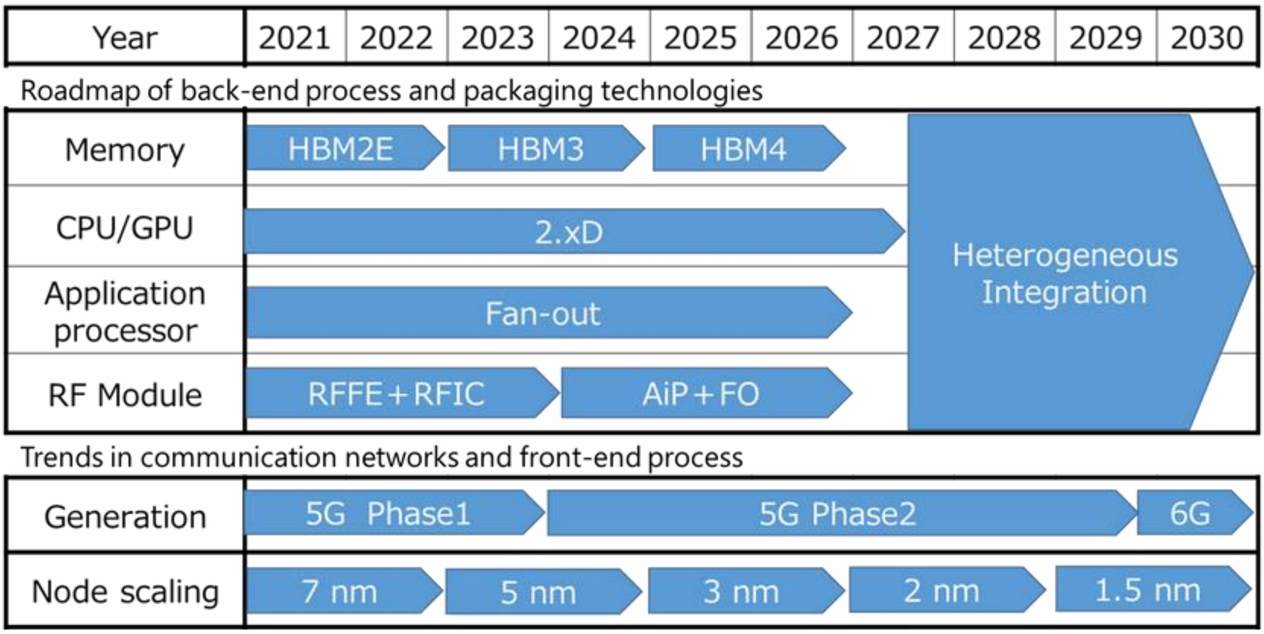
Telecommunications traffic is growing at an incredible pace with the continued development of future information societies envisioned with such initiatives as Germany's "Industrie 4.0," US General Electric's Industrial Internet, and "Society 5.0" proposed by Japan as well as the spread of IoT, 5G networks, ADAS, and generative AI in our everyday lives. Data centers are also processing a rapidly increasing volume of information. Flip chip-ball grid arrays (FC-BGA) currently serve as the mainstream substrates used for information processing devices in data centers, and are expected to see their quantities rise in the years ahead. The image below shows the applications of package (PKG) substrates and their market growth forecast.



02 | TECHNOLOGY ROADMAP

To respond to the expected explosive growth in information processing and transmission, data centers, communication modules, and edge terminals must be equipped with semiconductor devices capable of processing information more speedily in larger volumes and wider bandwidths. Meeting these needs will require an increasing number of semiconductors chips to be mounted by making these chips smaller and finer-pitched in the front-end process as well as advanced packaging (back-end process) technology to produce chips highly integrated and densely packed, thereby transmitting information at higher speeds and in wider bandwidths.

The demand is rising for more sophisticated back-end process technologies in response to advanced front-end process nodes, while expectations are heightening for high-integration technologies in the back-end process to overcome the limits of front-end process nodes. Consequently, there is a growing need for packaging technologies and package substrates with the capacity to respond to these higher performance requirements. The figure below shows a rough “roadmap of back-end process and packaging technologies” and the “trends in communication networks and front-end process technologies”



03 | TECHNOLOGY TRENDS TOWARD NEXT-GENERATION PACKAGING

Let us introduce specific technology trends toward higher-integration, higher-speed packaging technologies among other back-end technologies.

In the field of memory, the high bandwidth memory (HBM) standard has been put into practical use to increase information transmission speed, namely bandwidth, and to integrate more chips with memory chips stacked using through-silicon via (TSV) technology. An interface (I/F) chip with a processor is placed at the bottom of a standard four-layer memory, with these five chips interconnected by TSVs, that require vertical, fine-pitch connection accuracy.

In the HBM standard, the stacked memory is connected to the processor by a silicon (Si) interposer, which is a substrate used to conduct front and rear circuits with through-hole electrodes. First, both processor and memory are connected to an interposer (sub-substrate), and then the entire interposer is connected to a substrate. An Si interposer allows for a far larger amount of wiring than ordinary substrates, and provides higher information transmission speed due to its excellent electrical conductivity.

The technology of arranging in parallel, connecting, and packing multiple semiconductor chips using interposers, a common example of which is the combination of processors and memories, is referred to as 2.xD (dimensional) packaging. An increasing number of chips are expected to be mounted in the future in the pursuit of higher information transmission speed and integration.

Chiplet technology is being applied more and more as a packaging method using interposers. Chiplet technology is as follows; in order to improve the yields of large-scale single-integrated chip circuits, chips are split into multiple small chips and mounted on interposers to scale-up the circuits before being integrated into single packages. Combining processors with other chips can also help create a variety of specifications. Further combinations of chiplet represent one of the growing trends toward higher integration and speed.

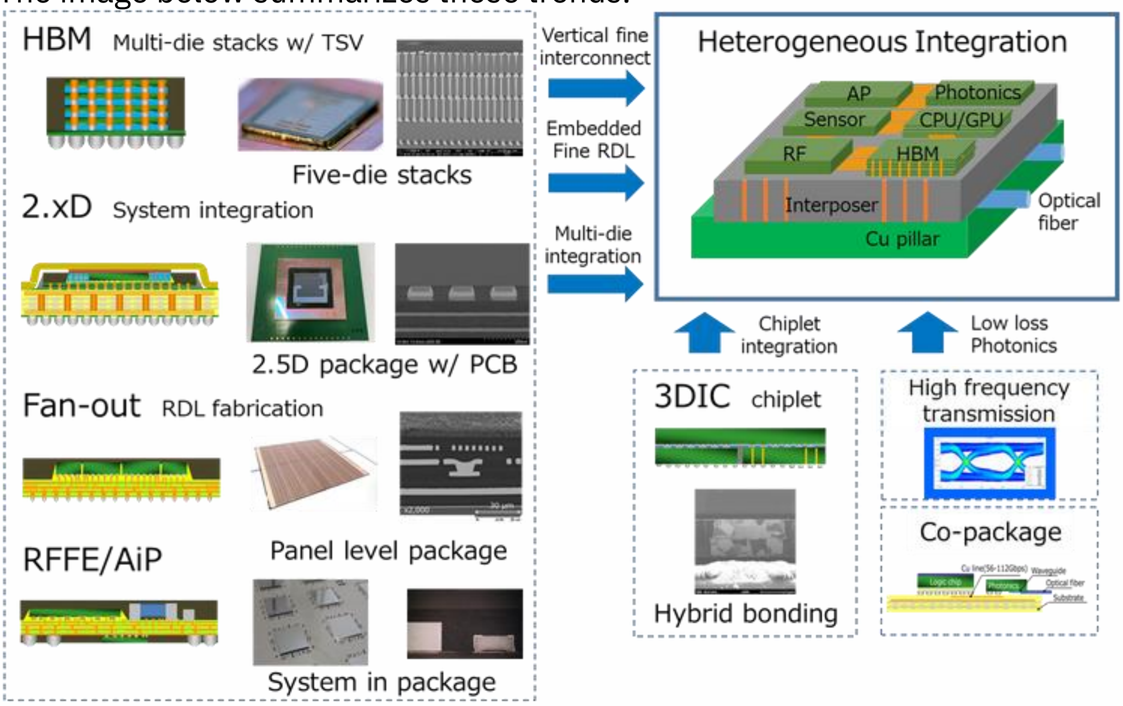
In terms of the technology for interconnecting semiconductor chips to printed wiring substrates, fan-out wafer-level packaging (FOWLP) is now used for application processors and other devices to connect with packages larger than the area of semiconductor chips. Redistribution layers (RDL) are formed on semiconductor wafers using wafer-level chip scale package (WLCSP) technology that forms wiring in a wafer state with semiconductor front-end process technology, thereby fanning out the terminals to the outside of the chips. RDL fabrication requires technologies for accurately embedding RDLs without distorting the surface flatness.

As a package in the wireless communication field, a radio frequency front-end (RFFE) module that integrates a power amplifier, high-frequency filter, RF switch, and low-noise amplifier is commonly used for the remote radio head (RRH: device transmitting and receiving radio signals) in a terminal. Antenna-in-package (AiP) integrating these modules with antennas is also being considered.

In these ways, next-generation semiconductor packages are progressing toward higher integration and speed through heterogeneous integration with different types of chips modularized and integrated into single packages.

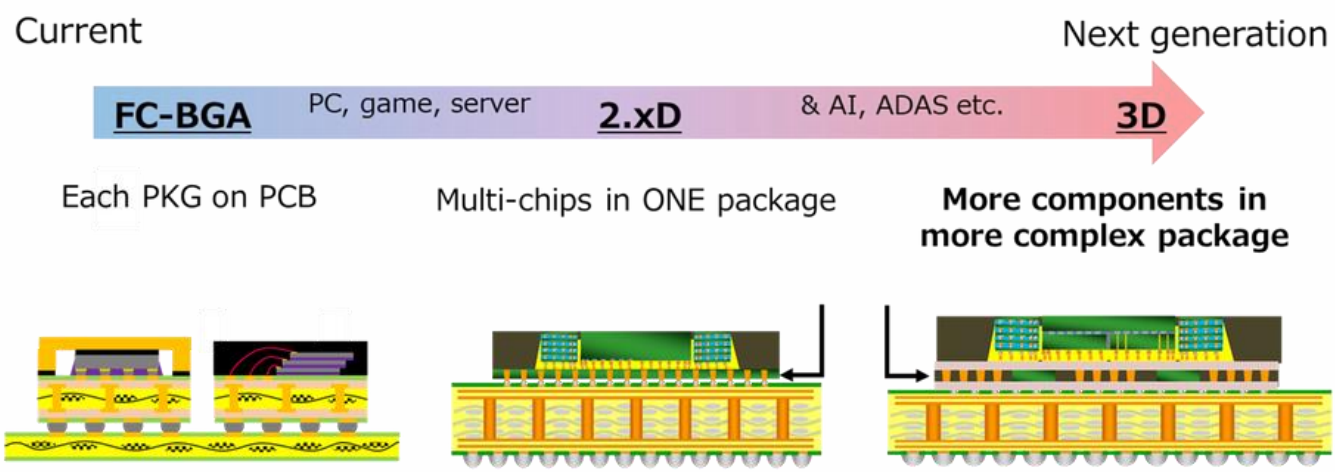
Amid these trends, development is fully underway to further advance 2.xD packaging to create 3D packaging technology for stacking and packaging multiple semiconductor chips, including memories and processors, in a three-dimensional direction, and even to combine 3D packages with three-dimensional integrated circuits (3DIC).

The image below summarizes these trends.



04 | 2.XD AND 3D PACKAGING

With semiconductor packaging shifting from the current FC-BGA to next-generation 2.xD and 3D packaging, the primary purpose of heterogeneous integration is to increase the bandwidth (speed) of the interconnection between the chips, thereby achieving higher integration. While chips and wires are becoming finer with smaller terminal intervals, packages are becoming larger with package substrates requiring larger areas, flatness, low warpage, and superior processability to support 3D packages.



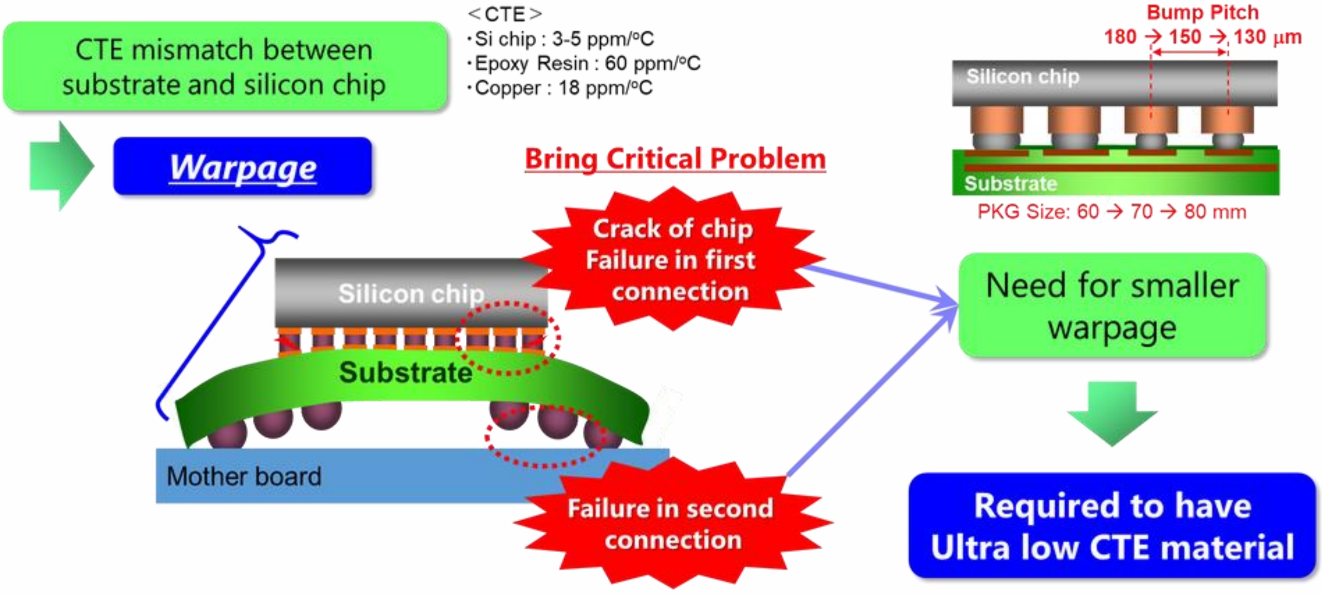
High bandwidth interconnect in backend process is the key technology for Heterogeneous integration

3. Properties required of core materials for next-gen. package substrates

01 | CHALLENGES OF 2.XD AND 3D PACKAGING: SUBSTRATE AREA ENLARGEMENT AND WARPAGE

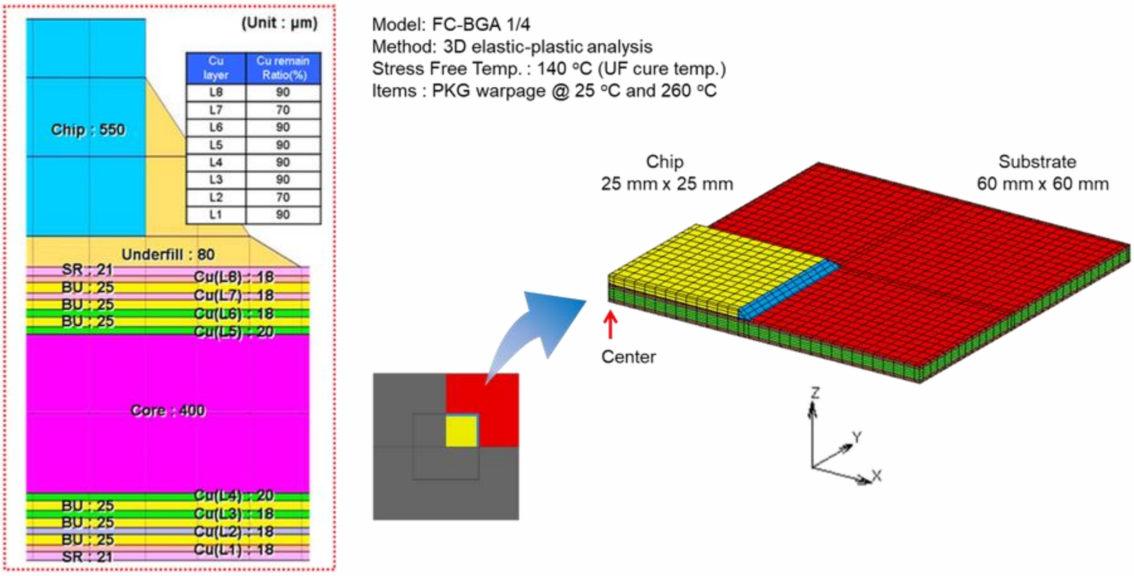
The core material of printed wiring boards (substrates) for packages is comprised of electrically conductive copper foil, electrical insulating resin and fillers, and glass cloth supporting the packaging components.

The coefficient of thermal expansion (CTE) varies greatly among Si chips, substrate resins, and copper foils. Heating and cooling with these different CTEs can cause fatal problems, such as substrate warpage, chip cracking, delamination in chip-to-package substrate connections, and connection failure between package substrates and motherboards. Next-generation packaging in particular requires substrates with smaller warpage, namely lower CTE, in response to narrower bump pitches and enlarged packages, or larger substrate areas.

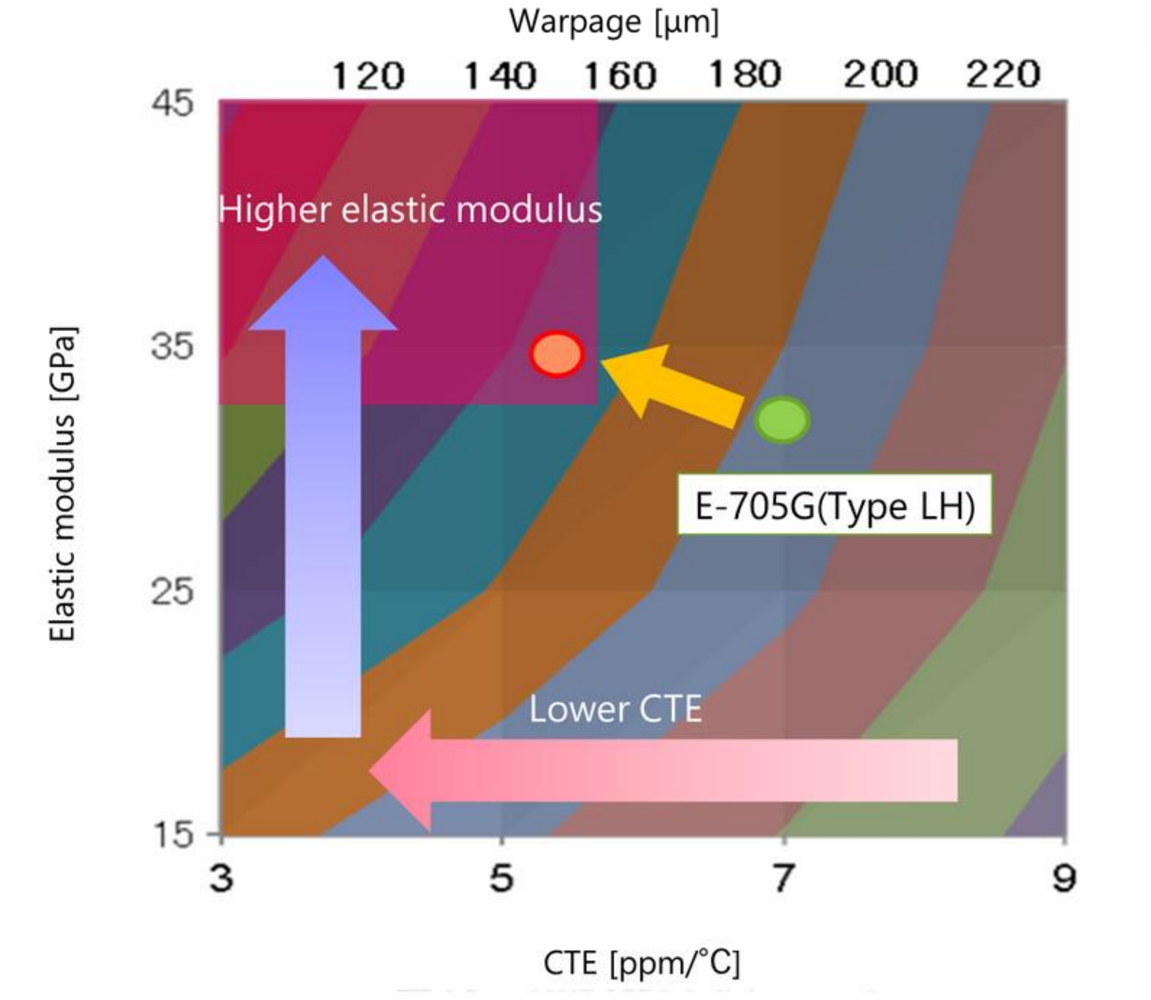


02 | CORE MATERIAL PHYSICAL PROPERTIES AND SUBSTRATE WARPAGE SIMULATION

Based on the FC-BGA structure shown in the figure below, Resonac simulated the amount of warpage at 25°C (cooling) and 260°C (reflowing) for a flat substrate at 140°C (underfill (UF) curing temperature) while changing the CTE and elastic modulus of the core material.



The simulation results shown in the figure below, with the same color belts representing the same warpage amounts, reveal that the substrate's warpage becomes smaller with lower CTE and higher elastic modulus. The results also show that both lower CTE and higher elastic modulus are required to develop even lower warpage materials than Resonac's relatively low-warpage E-705G(Type LH) among its conventional products.



03 | LOWERING CTE OF CORE MATERIALS

The approximate CTE of a composite core material is expressed in the Schapery equation. This expression shows that both CTE and elastic modulus of a resin system (including fillers) must be lowered to reduce the core material's CTE. As shown in the above simulation, higher elastic modulus is required for the entire core material to suppress substrate warpage, indicating the need to carefully balance lower elastic modulus for low CTE with higher elastic modulus for the entire core material.

Schapery equation (approximate expression of a composite material)

Resin | Glass cloth

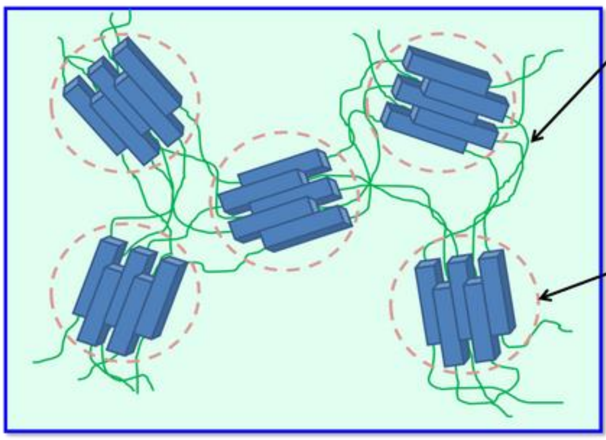
$$\alpha_{xy} \fallingdotseq \frac{\alpha 1E1V1 + \alpha 2E2V2}{E1V1 + E2V2}$$

α: CTE
V: Volume fraction
E: Elastic modulus
1: Resin
2: Glass cloth

α_{xy} : Method of lowering a substrate's CTE (x, y)

- *α_1 ⇒ Low* *(1) Lowering resin system's CTE (including fillers)*
- *E_1 ⇒ Low* *(2) Lowering resin system's elastic modulus*

Resonac uses its unique polymer blending technology to achieve both low elastic modulus for resin to lower a core material's CTE and high elastic modulus for the entire core material. In other words, hard segments with a rigid backbone of planar stacking structures contribute to the core material's lower CTE and higher elastic modulus, while soft segments with a flexible backbone of chain-like molecular structures help lower the core material's CTE and suppress residual stress by lowering the resin's elastic modulus. Each segment was optimally blended to realize both low CTE and high elastic modulus for the entire core material.



Soft segment (new flexible backbone)

Chain-like molecular structure
・Lower elastic modulus (lower CTE)
・Residual stress suppression

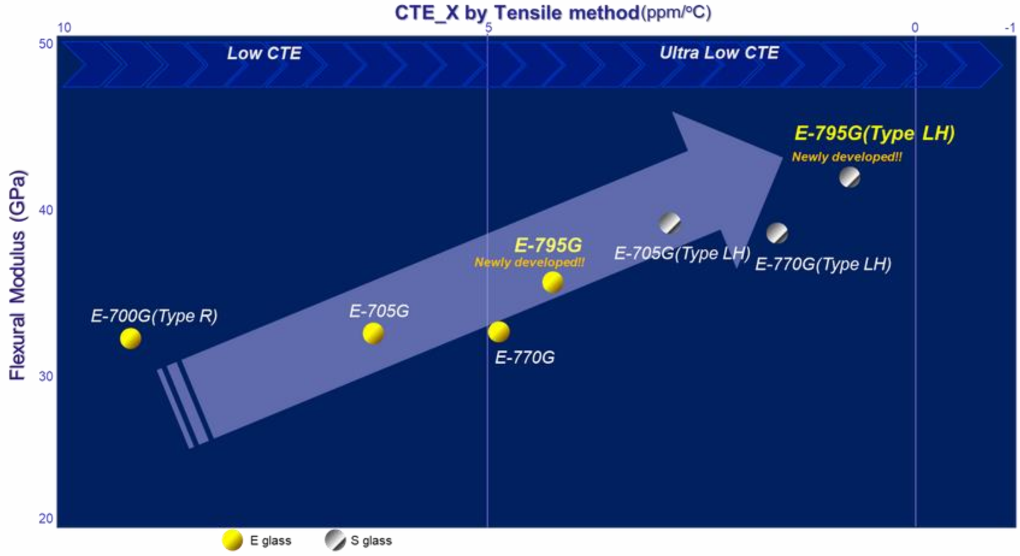
Hard segment (new rigid backbone)

Planar stacking structure
・Lower CTE
・Higher elastic modulus

4. Latest low CTE cores

01 | POSITIONING AND PROPERTIES OF E-795G AND E-795G(TYPE LH)

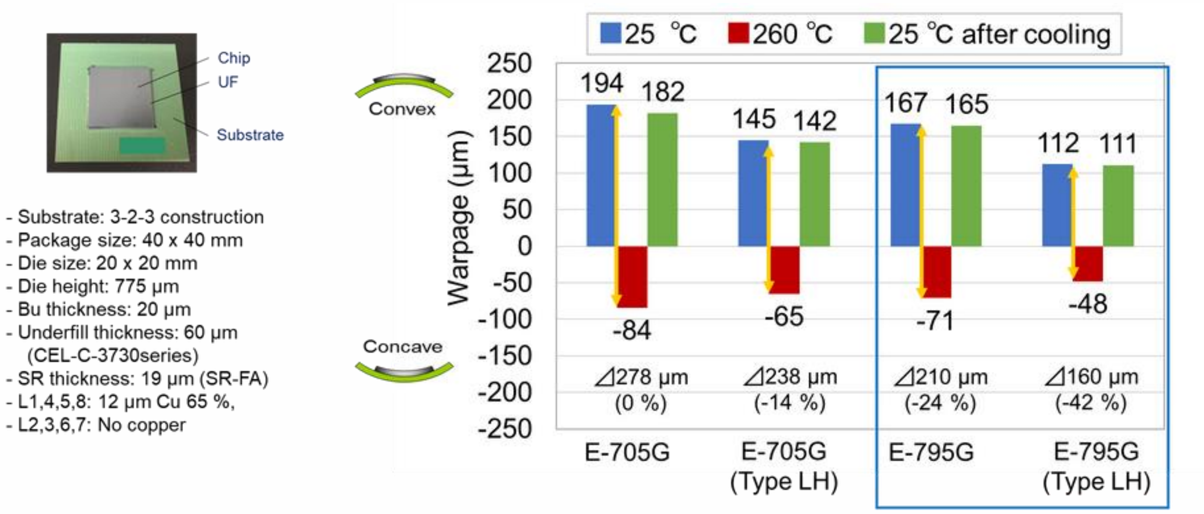
The realization of Resonac's newest core materials E-795G and E-795G(Type LH) is based on its development policies and ideas to suppress warpage while providing both low CTE and high elastic modulus. Type LH refers to the material with glass cloth. Both E-795G and E-795G(Type LH) achieve low CTE and high elastic modulus compared with our conventional E-705G, E-705G(Type LH), E-770G, and E-770G(Type LH). Resonac has successfully developed high elastic modulus, low CTE core materials by optimally blending hard and soft segments to apply low CTE resins, as mentioned earlier, and by increasing the volume of fillers.



Item	Conditions		E-705G	E-705G (Type LH)	E-795G	E-795G (Type LH)
Glass type	Glass type		E	S	E	S
	Weave density		Std.	High Density	Std.	High Density
Tg	TMA	°C	260	260	280	280
	DMA		300	300	330	330
Td(5%loss)	TGA	°C	440	440	480	480
CTE (Tensile)	α1(X,Y)	ppm/°C	5.9	2.8	4.0	0.7
Flexural Modulus	A	GPa	33	38	36	41
Elastic Modulus (DMA)	A	GPa	24	29	27	32
	260 °C		16	20	22	25
Peel Strength	12 μmSTD	kN/m	0.9	0.9	0.8	0.8
Dk	1 GHz (SPDR)	-	4.5	4.2	4.4	4.2
Df		-	0.008	0.008	0.006	0.006
Flammability	UL-94	-	Uncertified		**V-0 (t0.02~t1.61)**	

02 | EVALUATION OF WARPAGE IN PRIMARY PACKAGING

The figure below shows the warpage evaluation results during the primary packaging process. Resonac's E-795G and E-795G(Type LH) reduce warpage in packaging by 15% to 20% compared with its conventional E-705G and E-705G(Type LH), thereby achieving high insulation reliability.



03 | SIMULATION OF WARPAGE FOR CORE THICKNESS

The figures below show the warpage simulation results for the thicknesses of different core materials, with the amount of warpage expressed in values relative to the warpage of core material E-705G with 800 μm thickness as the benchmark. The thinner the core materials, the larger the warpage. If you want to thin the materials, E-795G(Type LH) maintains its warpage at a relative value of less than 1.0 even with its thickness reduced to 600 μm, as long as an acceptable relative value is below 1.0.

- Simulation method: 3D elastic analysis
  ΔWarpage: Difference between 25 °C and 260 °C
  Benchmark: E-705G 800 μm
- Simulation model
  - Substrate: 5-2-5 construction
  - Package size: 60 x 60 mm
  - Die size: 25 x 25 mm
  - Die height: 725 μm
  - Bu thickness: 30 μm
  - Underfill thickness: 80 μm (CEL-C-3730S-012L3-20)
  - SR thickness: 20 μm (SR7300)
  - Cu thickness: 18 μm
  - Cu coverage: 80%

Core thickness (μm)	ΔWarpage index			
	E-705G	E-705G (Type LH)	E-795G	E-795G (Type LH)
200	2.13	1.91	1.95	1.76
400	1.61	1.36	1.43	1.17
600	1.24	1.00	1.08	0.79
800	**1.00**	0.78	0.84	0.61
1000	0.87	0.61	0.69	0.48
1200	0.68	0.49	0.54	0.38
1400	0.57	0.41	0.46	0.31
1600	0.49	0.34	0.39	0.26

- Simulation method:
  3D elastic analysis
  Benchmark: E-705G 800 μm
- Simulation model
  - Substrate: 5-2-5 construction
  - Package size: 60 x 60 mm
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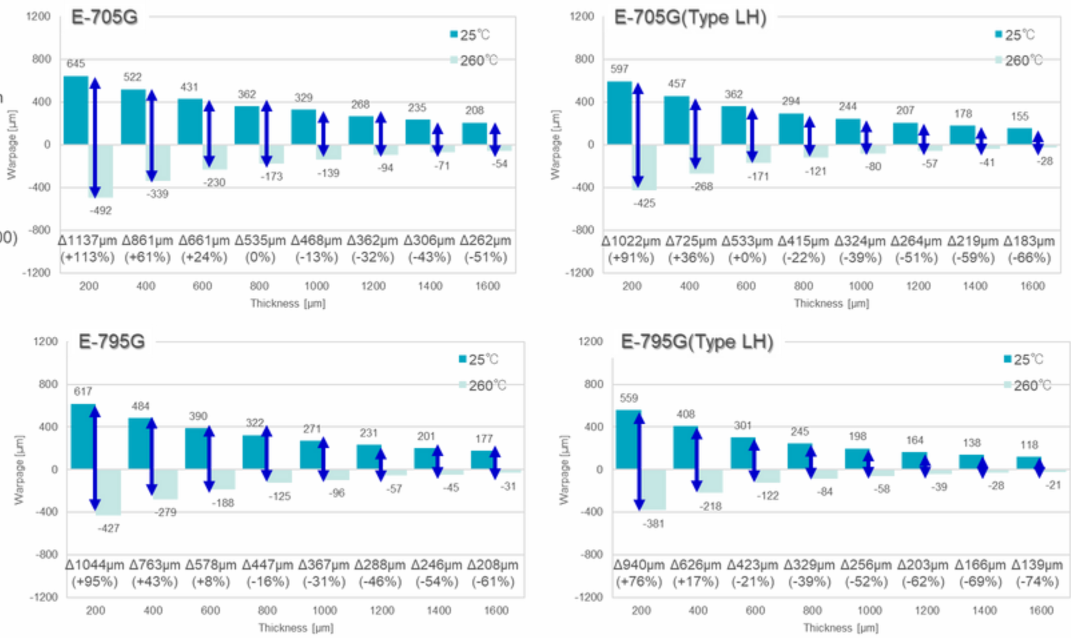
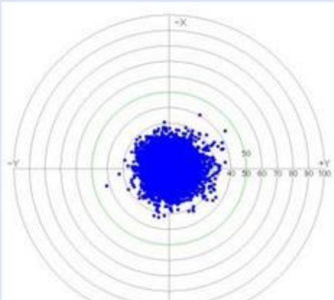
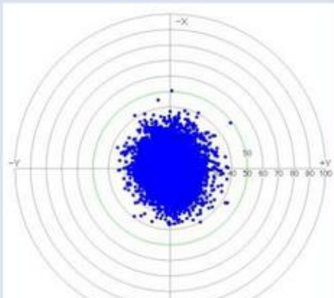
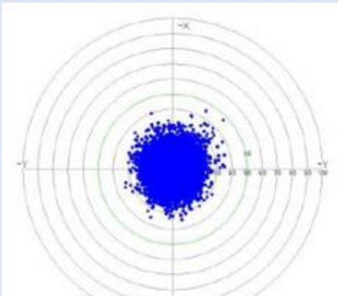
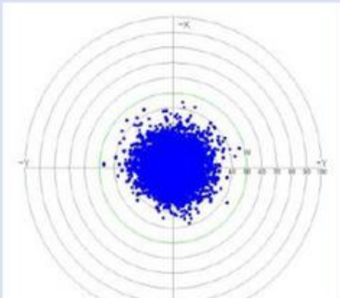


04 |DRILLING PROCESSABILITY

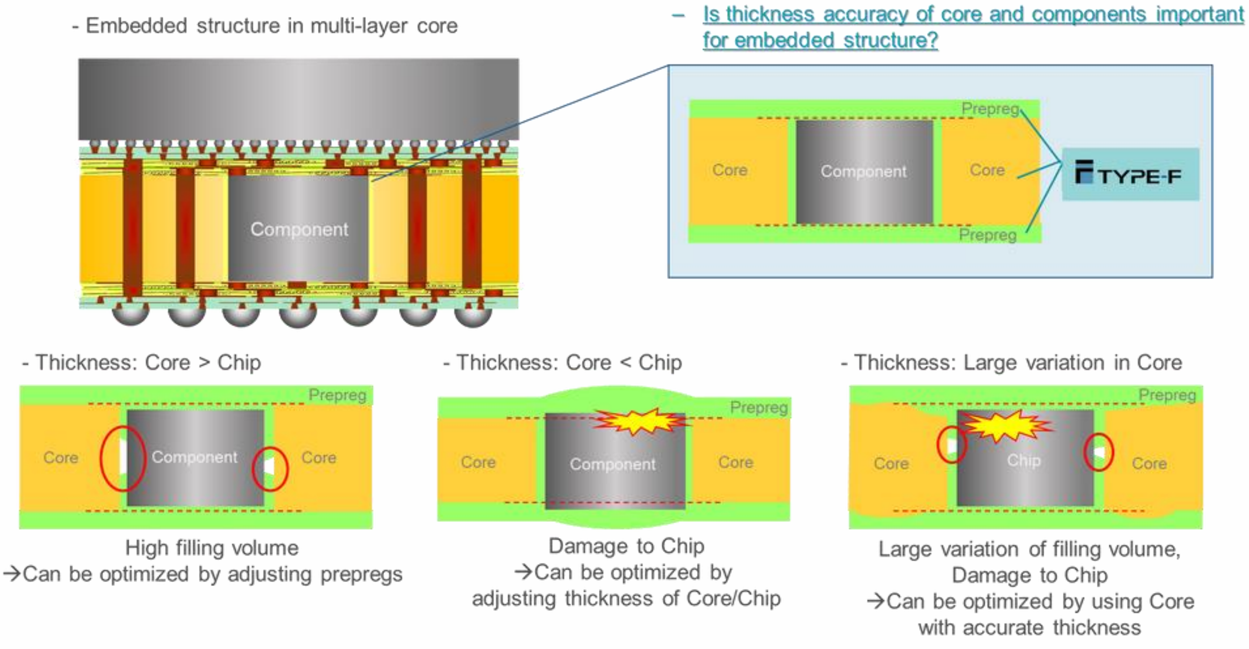
E-795G is a core material with high elastic modulus. Its drilling processability, including variation in hole position accuracy, is equivalent to our conventional products.

Item	Type	
	-	Type LH
E-705G	 Ave+3σ：26.4 μm	 Ave+3σ：35.6 μm
E-795G	 Ave+3σ：29.6 μm	 Ave+3σ：37.6 μm

5. TYPE-F technology in pursuit of flatness and thickness accuracy

01 | NECESSITY OF CORE MATERIALS WITH HIGH THICKNESS ACCURACY

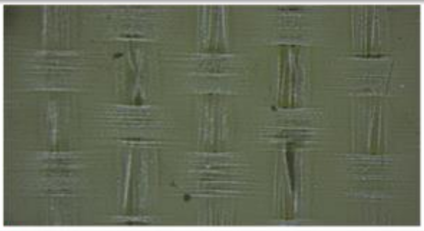
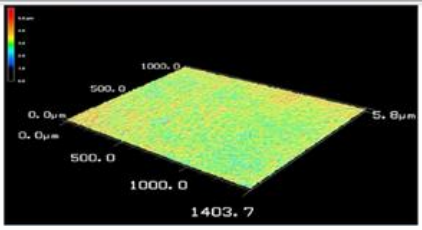
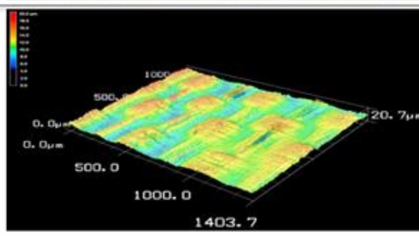
High thickness accuracy is required to ensure connection reliability during the packaging process. Component-embedded substrates especially require thickness accuracy for cores and components since thinner cores or uneven thicknesses are likely to damage the components.



02 | INTRODUCTION OF TYPE-F TECHNOLOGY

Resonac’s TYPE-F technology, an upgraded version of E-705G and E-705G(Type LH), pursues both higher thickness accuracy and flatness using the same core material.

- Features
  - Smooth surface
  - Small thickness variation
  - Good filling capability
  - Stable dimension change

Item	TYPE-F	Normal type
Prepreg surface		
Laser microscope (KEYENCE, VK-X100)		

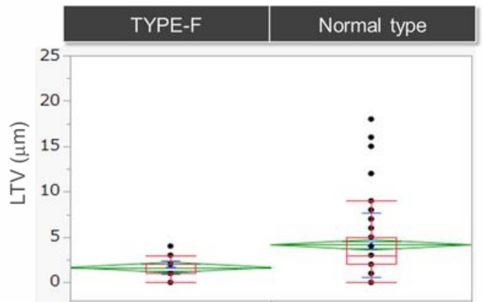
TYPE-F technology can uniformly coat the resin on the glass cloth

03 | TYPE-F CORE PROPERTIES (THICKNESS ACCURACY, DIMENSIONAL CHANGE, WARPAGE)

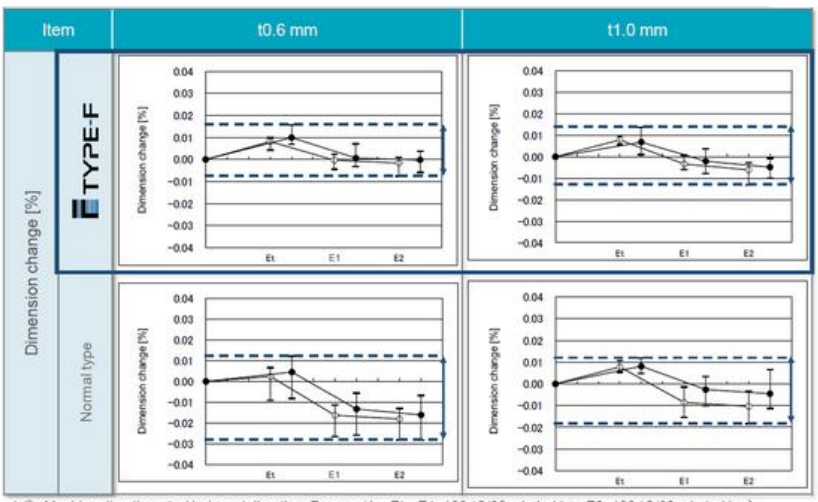
Thickness accuracy of TYPE-F core and conventional type was compared by measuring thickness variation within a 1-meter-square board. Thickness variation was also measured after etching and baking, and when assembling laminated substrates for packaging. The results are shown in the figures below.

As seen in the figures, TYPE-F core produced smaller variations than the conventional type in terms of board thickness, dimensions after processing, and thickness as a package substrate.Core materials with high thickness accuracy contribute to improved connection reliability of component-embedded substrates and bump connections.

■ Material: E-705G(Type LH) t1.0 mm (78 points: 26 points x 3 lot)



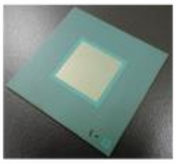
	TYPE-F	Normal type
LTV Ave [µm]	1.7	4.1
LTV Std. [µm]	0.9	3.5
LTV Max [µm]	4	18
Student's t-Test	Significant Difference (P value <0.001)	



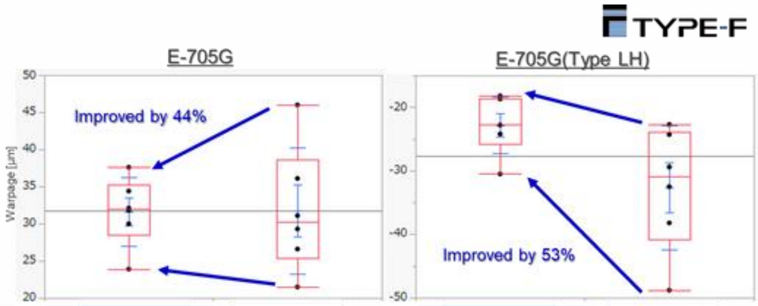
TYPE-F

* ○: Machine direction, ●: Horizonal direction, Process(A→Et→E1: 180 °C/60 min baking, E2: 180 °C/60 min baking)

- Type-F core had smaller variation of the dimension change than Normal-type core in both thicknesses t0.6 and t1.0 mm.



- Substrate: 6-2-6 construction
- Package size: 60 x 60 mm
- Core thickness: 1.2 mm
- Bu thickness: 30 µm
- SR thickness: 20 µm (SR-7400)
- L1, 14: 18 µm Cu 65 %
- L3, 5, 10, 12: 18 µm Cu 100%
- L7, 8: 12 µm Cu 100%
- L2, 4, 6,9, 11, 13: No copper



	E-705G		E-705G(Type LH)	
Item	TYPE-F	Normal type	TYPE-F	Normal type
Warpage Variation (µm) (25 °C)	13.7	24.5	12.3	26.1
Improvement rate (%)	44	-	53	-

– Type-F core had smaller variation of Bare substrate warpage than Normal-type core.

As described above, next-generation semiconductor package substrates require larger areas to accommodate multiple devices and support future 2.xD and 3D packaging, and their core materials need to provide low CTE and high elastic modulus to achieve low warpage as well as high thickness accuracy to ensure connection reliability during the packaging process.

In response to these demands, Resonac has developed the core material MCL-E-795G with low CTE and high elastic modulus by applying low CTE resin and increasing the volume of fillers. MCL-E-795G reduces warpage in packaging by 15% to 20% compared with our conventional types. In addition, Resonac’s TYPE-F technology for accurate thickness cores contributes to improved connection reliability of bump connections.

* “MCL” is Resonac Corporation’s registered trademark in Japan, the United States, Italy, Canada, Singapore, France, Benelux, Poland, Malaysia, Mexico, South Korea, Hong Kong, Taiwan, and China.
* “TYPE-F” is Resonac Corporation’s registered trademark in Japan.

About us

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Showa Denko and Showa Denko Materials (formerly Hitachi Chemical) merged and became a new company, Resonac.

The Resonac Group is a group of chemical companies that produces and sells products related to semiconductor and electronic materials, mobility, innovation enabling materials, chemicals, etc. The Group has a wide variety of materials and advanced material technologies applicable to midstream to downstream of supply chains of various products. In January 2023, the Showa Denko Group and the Showa Denko Materials Group (former Hitachi Chemical Group) merged into the Resonac Group and made a start as a new corporate group. The new trade name “RESONAC” was created as a combination of two English words, namely, the word of “RESONATE” and “C” as the first letter of CHEMISTRY. As a “co-creative chemical company,” Resonac aims to continue growing and enhance its corporate value through co-creation. The Group recorded net sales of about 1,400 billion yen in 2022, and its overseas sales accounted for 56% of net sales. The Group has deployed production/sales bases in 22 countries and regions, and continues operating its business globally (as of January 2023).

For detail, please refer to our Website.

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RESONAC

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