HDI Stackup Guide

Layer stackup recommendations for 4 to 12+ layer HDI boards, including impedance targets, via strategy, and material selection considerations.

Prepared by Electuni LLC • Circuit Board Design • circuit-board-design.com

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This guide helps you choose practical HDI layer stackups and via strategies, and communicate clear requirements to your fabricator. It focuses on repeatable, production-oriented choices rather than one-off hero builds.

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Key terms

- **HDI**: High Density Interconnect; uses fine-line routing and microvias (laser-drilled) to increase routing density.
- **Microvia**: Laser via, typically connecting adjacent layers (L1-L2, L2-L3). Often stacked or staggered.
- **Sequential lamination**: Building the PCB in stages (adds cost and risk). Notation: 1+N+1, 2+N+2, etc.
- **Via-in-pad (VIP)**: Via placed in a component pad, usually filled and capped (common under BGAs).

When to use HDI

- Fine-pitch BGAs (0.8 mm and below), high pin-count SoCs/FPGAs, dense RF modules.
- Tight form factors where fanout and routing channels are limited.
- High-speed buses needing short stubs and controlled reference transitions.
- When standard through-vias would consume too much area or force extra layers.

Design inputs to lock early

- Target impedance(s) and tolerance (e.g., 50 ohm SE, 90/100 ohm diff) and reference plane assignment.
- BGA pitch, escape strategy (dogbone vs via-in-pad), and allowable assembly processes.
- Fabricator capability: min trace/space, laser via size, via fill/cap options, registration class.
- Material selection (FR-4 vs low-loss) driven by frequency/data rate and cost.

Common HDI stackup patterns

These are the most common, cost-effective patterns. Exact thicknesses depend on fab/material and impedance needs.

Pattern	Use case	Notes
1+N+1	Entry HDI (6-10 layers total)	Microvias on outer build-up layers; core uses through-vias. Good co
2+N+2	Higher density / finer BGAs	More build-up layers increase routing channels; more lamination cy
Any-layer via	Maximum density	Microvias can connect any adjacent layer; highest cost and process

Example reference stackups

Use these as communication templates. Your fab will replace thickness/material with their catalog while meeting impedance.

4-layer (standard, non-HDI) - baseline reference

Layer	Function	Notes
L1	Signals	High-speed on L1 with solid L2 reference where possible.
L2	GND plane	Continuous reference plane; minimize splits.
L3	Power / signals	Power islands; route slower signals; keep return paths in mind.
L4	Signals	External signals; consider GND pour where beneficial.

8-layer 1+6+1 (common HDI starting point)

Layer	Function	Notes
L1	Signals	Microvia fanout from BGAs; controlled impedance routes.
L2	GND plane	Primary reference for L1; dense stitching around transitions.
L3	Signals / power	Short runs, escape channels; avoid long reference breaks.
L4	GND plane	Reference for L3/L5 where needed; helps EMC.
L5	Signals / power	Internal routing channels; keep high-speed grouped.
L6	GND or power	Plane layer; choose based on PDN needs.
L7	GND plane	Reference for L8; supports clean returns.
L8	Signals	Bottom escape and routing; keep critical nets short.

10-layer 2+6+2 (higher density, more routing channels)

Layer	Function	Notes
L1	Signals	VIP/microvia fanout, controlled impedance.
L2	GND plane	Primary reference.
L3	Signals	Second build-up routing channel.
L4	GND plane	Reference and shielding.
L5	Signals / power	Core routing.
L6	Power plane	Dedicated PDN layer (or split across L5/L6).
L7	Signals / power	Core routing.
L8	GND plane	Reference and shielding.
L9	Signals	Build-up routing channel.
L10	Signals	Bottom routing and escape.

Via strategy guidelines

- Prefer **staggered microvias** for yield. Use **stacked** only when routing density demands it and the fab supports it.
- For BGAs, choose between **dogbone escape** (lower cost) vs **via-in-pad** (higher density). If VIP: specify **filled and capped** to prevent solder wicking.
- Limit via types: keep a small set of laser via sizes and core drills to simplify fabrication.
- Minimize stubs on high-speed nets: use blind/buried vias, backdrill, or shorter layer transitions when warranted.

Impedance and dielectric notes

- Controlled impedance depends on trace geometry, dielectric thickness, copper roughness, and resin content. Use the fabricator's field solver outputs as the source of truth.
- Keep return paths continuous: avoid splits under high-speed routes; add stitching vias at layer transitions.
- For high data rates, consider lower-loss laminates and tighter impedance tolerance; cost increases with material and process control.

What to send to the fabricator (HDI order clarity)

- Requested stackup pattern (e.g., 1+6+1) and layer functions (signal/plane).
- Impedance table: nets, targets, tolerance, reference layer, and test coupon requirement.
- Microvia requirements: laser via diameter, pad diameter, whether stacked or staggered, and VIP fill/cap spec (if used).
- Finish and assembly constraints: ENIG vs ENEPIG (often for fine-pitch), mask type, and any microvia tenting rules.
- Special processes: backdrill, edge plating, controlled depth, sequential lamination count.

Practical reminder

HDI success is mostly about disciplined constraints and early fab alignment. Choose the simplest stackup that meets routing density and signal integrity, then build robust documentation so your fabricator can hold impedance and registration predictably.