PCB DFM Checklist

A comprehensive Design for Manufacturability checklist covering routing rules, via strategy, solder mask/paste, panelization, and release documentation.

Prepared by Electuni LLC • Circuit Board Design • circuit-board-design.com

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Design for Manufacturability (DFM) is the discipline of making layout decisions that reduce fabrication and assembly risk. Use this checklist during layout and again before release to lock a clean, production-ready handoff.

Revision: 1.0 • Date: 2026-02-09

Scope and assumptions

- Applies to rigid FR-4 PCBs unless otherwise specified.
- Targets below are typical; always confirm with your selected fabricator and assembler.
- For high-speed, high-voltage, or safety-critical products, treat this as a baseline and add project-specific rules.

Pre-layout decisions

Lock these before routing. Most DFM failures originate from late stackup or footprint changes.

- Stackup defined (layer count, copper weights, dielectric thicknesses) and agreed with fab.
- Impedance requirements defined (single-ended / differential, tolerance, reference planes).
- Fabrication class agreed (standard vs fine-line vs HDI) and minimums documented.
- Assembly process agreed (reflow vs wave/selective, lead-free), conformal coat (if any), and test strategy.
- Footprints validated against datasheets and supplier land-pattern guidance.

Core fabrication rules checklist

Area	What to verify	Typical targets / notes (confirm with fab)
Trace / space	All nets meet minimum trace width/spacing; critical nets use controlled rules.	Standard: 4/4 mil (0.10/0.10 mm). Fine-line: 3/3 mil. Keep extra m
Copper to edge	No copper features too close to board edge or cutouts.	Common: >= 10 mil (0.25 mm) copper-to-route; more for castella
Drill sizes	Finished hole sizes available; drills not below fab capability.	Common PTH >= 0.20-0.25 mm finished. Avoid too many unique
Aspect ratio	Plated through-hole aspect ratio within capability.	Rule of thumb: thickness / drill <= 8:1 to 10:1 for standard yields.
Annular ring	Pads provide adequate annular ring after registration tolerances.	Typical external annular ring >= 4 mil; internal >= 3-4 mil. Higher
Via-to-copper	Clearance rules for drills to copper pours/tracks.	Typical 6-8 mil clearance; include anti-pad sizing for planes.
Solder mask	Mask slivers avoided; mask expansion tuned; tent vias when needed.	Minimum mask dam often ~4 mil. Verify mask expansion and via
Silkscreen	Silk does not print on pads; reference designators readable.	Keep silk >= 4-6 mil from exposed copper. Use consistent polarit
Plane splits	Return paths not broken; stitching vias around transitions.	Avoid routing critical signals across plane gaps; keep reference c
Thermals	Thermal relief and spoke widths suitable for assembly.	Avoid direct-connect to large pours for small passives unless req

Area	What to verify	Typical targets / notes (confirm with fab)
Copper balance	Copper distribution balanced to reduce warpage and etch issues.	Use thieving/pours; check each layer for large unbalanced areas

Assembly and reliability checklist

bullet Component courtyard clearances meet assembly house requirements (especially around BGAs, connectors, tall parts).

bullet Solder paste apertures reviewed for fine-pitch parts, QFNs, and large thermal pads (window-pane where needed).

bullet Via-in-pad only when required; specify via filling/capping if used under BGAs/QFNs.

bullet Thermal pad strategy defined (stitch vias, via tenting, paste reduction) to prevent voiding and float.

bullet Fiducials present (global and local) and defined in fab notes.

bullet Test points provided for power rails, programming, and key nodes; spacing compatible with probes/fixtures.

bullet Clear polarity/orientation markers for diodes, electrolytics, IC pin-1, connectors, LEDs.

Panelization and tooling

bullet If panelized: rail width, breakaway method (mouse-bites / V-score), and tab locations defined.

bullet Tooling holes and fiducials added on panel rails (or specify assembler-managed panelization).

bullet Keepout zones for depanel tools and conveyors considered (edge clearance for tall parts).

bullet For RF: controlled edge plating, via fences, and keepouts specified if required.

Release package

bullet Gerbers/ODB++/IPC-2581 plus drill files (PTH/NPTH separated) and a short readme.

bullet Stackup table including materials, copper weights, dielectric thickness, impedance callouts.

bullet Fabrication drawing: outline/cutouts, tolerances, finish (ENIG/HASL), mask/silk colors, controlled impedance, special processes (edge plating, via fill/cap).

bullet Assembly package: BOM with manufacturer part numbers, assembly drawing, centroid file, and any programming/test instructions.

bullet Netlist and DRC report snapshot; document any intentional exceptions.

Final sign-off

Run DRC/ERC, perform a full 3D and clearance review, and do a short peer review focused on the items above. If possible, request a fab DFM review and address findings before the first build.